Semester 2

Logic System Design

Course Code	Teaching hours per week				Credits	Exam hours	Course type	CIE Marks	ESE Marks
	L	T	P	R					
26NLNPC201	2	1	0	0	3	2.5	PCC	40	60

1. **Preamble:** This course provides a comprehensive introduction to digital electronics, covering number systems, logic gates, Boolean algebra, and the analysis and design of combinational and sequential circuits. It also introduces state machines, data conversion techniques, and basic hardware description using Verilog, forming a strong foundation for digital system design.
2. **Prerequisites:** Basic knowledge of elementary mathematics and fundamental electrical/electronic concepts is required. Familiarity with algebraic operations and logical reasoning will help in understanding the course content.

Module Number	Syllabus Description	Contact Hours
1	Number Systems and Codes – binary, octal and hexadecimal – conversions – ASCII code, Excess – 3 code, Gray code, BCD code. Signed numbers – 1's complement and 2's complement – addition and subtraction. Basic logic gates – universal gates – Boolean laws and theorems – Sum of products and Product of sums form. K map representation and simplification (up to four variables) – pairs, quads, octets – don't care conditions.	12
2	Combinational circuits – half adder and full adder, half subtractor and full subtractor – 4-bit parallel binary adder/subtractor. Comparators – parity generators and checkers – encoders – decoders – BCD to seven segment decoder. Multiplexers – implementation of boolean expressions using multiplexers – demultiplexers.	12
3	Flip-Flops – SR, JK, D and T flip-flops – characteristic table and excitation table – JK Master Slave Flip-flop – Conversion of flip- flops – SR to JK and JK to SR only. Up/Down counters – asynchronous counters – mod-6 and mod-10 counters. Synchronous counters – design of synchronous counters – Ring counter – Johnson Counter. Shift registers - SISO, SIPO, PISO, PIPO.	14
4	State Machines – state transition diagram – Moore and Mealy machines.	10

	Digital to Analog converter – weighted resistor type, R-2R Ladder type. Analog to Digital Converter – flash type, successive approximation type. Introduction to Verilog – Implementation of AND, OR, half adder and full adder.	
	Total hours	48

3. Course Assessment Method (CIE: 40 Marks, ESE: 60 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions.

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks (8x3 =24marks)	● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 subdivisions. (4x9 = 36 marks)	**60**

4. Course Outcomes

At the end of the course students should be able to:

Course Outcomes		Blooms Taxonomy Level
CO1	Identify various number systems, binary codes and formulate digital functions using Boolean algebra.	K3
CO2	Design combinational logic circuits.	K3
CO3	Design sequential logic circuits.	K3
CO4	Describe the operation of various analog to digital and digital to analog conversion circuits.	K2
CO5	Explain the basic concepts of programming using Verilog HDL.	K2

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyze, K5- Evaluate, K6- Create

5. Mapping of Course Outcomes with Program Outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	2									3
CO2	3	2	2	2							3
CO3	3	2									3
CO4	3	2									3
CO5	3	2			2						3
CO6	3	2									3

6. Text Books

Sl No	Title of Book	Name of Author/s	Publisher	Edition and Year
1	Digital Fundamentals	Floyd T.L	Pearson/Prentice Hall, 11th	Edition, 2015 / Global Edition 2025 (latest)
2	Digital Principles and Applications	Albert Paul Malvino & Donald P. Leach	McGraw-Hill Education / Tata McGraw-Hill Education,	8th Edition, 2015
3	Digital Systems: Principles and Applications	Ronald J. Tocci, Neal Widmer, Gregory Moss	Pearson Education	12th Edition , 2022

7. Reference Books

Sl No	Title of Book	Name of Author/s	Publisher	Edition and Year
1	Fundamentals of Digital Circuits	A. Ananda Kumar	PHI Learning,	4th Edition, 2016
2	Digital Logic and Verilog HDL Fundamentals	Joseph Cavanagh	CRC Press, 1st Edition,	2008/2017
3	Digital Design: With an Introduction to the Verilog HDL	M. Morris Mano & Michael D. Ciletti	Pearson, 6th Edition,	2017/2018

8. Video Links or any other Reference Materials

Sl No	Details Like Weblink, Publication Details	Module
1	https://youtube.com/playlist?list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX&si=QHK0wOMwBx0viVTG	1
2	https://youtube.com/playlist?list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX&si=QHK0wOMwBx0viVTG	2

3	https://youtube.com/playlist?list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX&si=QHK0wOMwBx0viVTG	3
4	https://youtube.com/playlist?list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX&si=QHK0wOMwBx0viVTG	4

MODEL QUESTION PAPER

FEDERAL INSTITUTE OF SCIENCE AND TECHNOLOGY
(Autonomous)
SECOND SEMESTER B.TECH DEGREE EXAMINATION (2026 Scheme)

Course Code: 26NLNPC201
Course Name: Logic Systems Design

Max Marks: 60 **Duration: 2 Hours 30 minutes**

PART-A
(Answer all Questions, Each Question Carries 3 Marks)

1		Convert l0l10010 to hexadecimal and Octal	CO1	3
2		Subtract decimal number 22 from 17 using 8 bit 2's complement method.	CO1	3
3		Using the Boolean laws and rules, simplify the logic expression $Z = (\bar{A}+B)(A+B)$	CO2	3
4		Derive the expression for sum and carry of a full adder	CO2	3
5		Determine the number of flip-flops needed to construct a register capable of storing (i) a 6 bit binary number (ii) hexadecimal numbers upto F (iii) octal numbers upto 10.	CO3	3
6		What are the asynchronous inputs of a flip flop? Why are they called so?	CO3	3
7		Differentiate between Moore and Mealy state machines.	CO4	3
8		Draw the circuit of flash ADC and explain.	CO4	3

PART-B **(Answer any one full Question from each Module, Each Question Carries 9 Marks)**				
9	a	Convert the following i) (1001011)gray = ( )2 ii) (10110110.0011)2 = ( )BCD iii) (5762)8 = ( )16 iv) (76)10 = ( )gray v)Attach the proper even parity bit to 10100100 and odd parity bit to 11111000.	CO1	5
	b	What are universal gates? Why are they called so?	CO1	4
OR				
10	a	With example explain any two representations for signed binary numbers	CO1	5
	b	Obtain the simplified POS expression using K- map Y =Σm (I,3,7,11,15) + d (0,2,4)	CO1	4
11	a	Design and draw implementation circuit for an odd parity generator circuit for 4bit binary data.	CO2	5
	b	Design and set up a half adder/subtractor circuit with mode control.	CO2	4
OR				
12	a	Design and set up a Binary to BCD converter circuit	CO2	5
	b	Draw the implementation circuit of a 1 : 8 Demultiplexer using two 1 : 4 demultiplexers	CO2	4
13	a	Illustrate the conversion of (a) a J-K flip-flop into a D flip-flop and (b) a J-K flip-flop into a T flip-flop. Explain.	CO3	4
	b	What is modulus of a counter? Draw the circuit of an asynchronous decade counter.	CO3	5
OR				
14	a	Draw the logic diagram of a 4-bit Johnson counter which employs D flip-flops. Write down its count sequence table and draw the timing diagram.	CO3	4

	b	Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 3, 5, 7, 6, 2, 1, ...	CO3	5
15	a	Explain the working of successive approximation ADC with the help of an example.	CO4	5
	b	Give the Verilog code for Half adder	CO4	4
OR				
16	a	With the help of a neat circuit diagram, explain how a R-2R ladder type DAC converts a digital signal to analog signal.	CO4	5
	b	Give the Verilog code for AND gate	CO4	4