Course Code & Name	26CAPC2001 Computer Organization & Architecture		
Teaching Hours /week (L: T:P: R)	3:1:0:0	Credits	4
CIE Marks	40	ESE Marks	60
Course Type	Theory (PCC)	Exam Hours	3
Prerequisites (if any)	26CAPC1003		

Course Objectives:

1. To develop a foundational understanding of the basic structure and functioning of computer systems.
2. To apply concepts of microarchitecture, pipelining, and memory hierarchy for improving system performance.
3. To understand input/output organization, interrupts, DMA, and bus arbitration mechanisms in computer systems.
4. To introduce advanced computer architecture concepts such as NPUs, unified memory architectures, and parallel processing techniques.

Course Outcomes (COs)

At the end of the course, students should be able to:

CO#	Course Outcomes	Bloom's Knowledge Level (KL)
CO 1	Apply the concepts of computer organization, instruction formats, addressing modes, and arithmetic operations.	3
CO 2	Apply microarchitecture concepts in processor organization, control unit design, instruction set architecture, and pipelining.	3
CO 3	Explain the organization of memory hierarchy, cache memory, virtual memory, interrupts, and I/O operations.	2
CO 4	Apply advanced computer architecture concepts including NPUs, unified memory, pipelining, and parallel processing.	3

Note: *K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

CO #	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8
CO 1	3	3	2	2	-	-	-	1
CO 2	3	3	3	3	1	-	-	2
CO 3	3	2	1	3	-	-	-	1
CO 4	2	2	1	2	-	-	-	2

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), - : No Correlation*

Course Assessment Method

(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE)

Attendance	Assignment/ Micro-project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
8	12	10	10	40 Marks

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions.

PART A	PART B	TOTAL
■ 2 Questions from each module. ■ Total of 8 Questions, each carrying 3 marks **(8x3 =24 marks)**	■ Each question carries 9 marks. ■ Two questions will be given from each module, out of which 1 question should be answered. ■ Each question can have a maximum of 3 subdivisions. **(4x9 = 36 marks)**	**60 Marks**

SYLLABUS

Module #	Syllabus Description	Hours
1	**Basic Structure of Computers:** Basic Operational Concepts, Bus Structures, Instructions and Instruction Sequencing–Instruction Types, Instruction Execution and Straight Line sequencing, Branching. **Arithmetic & Logic Unit:** Design of Fast Adders- Carry Look Ahead Addition, Multiplication of Positive Numbers, Signed Operand Multiplication (Booth's algorithm).	**12**
2	**Basic Processor Organization:** CPU structure and functions, Instruction format, types, and execution cycle, RISC vs. CISC architectures, Register organization. **Control Unit Design:** Hardwired control, Microprogrammed control, Design of control unit, Control memory and address sequencing. **Instruction Set Architecture (ISA):** Characteristics of instruction sets, Addressing modes, Instruction types - Data transfer, arithmetic, logical, control, I/O, Examples of typical instruction set architecture.	**12**
3	**I/O Organization:** Accessing I/O Devices, Interrupts–Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices. Direct Memory Access, Bus Arbitration. **Memory Organization:** Introduction to memory hierarchy, Cache memory - Organization, mapping techniques, replacement algorithms, Virtual Memory: Paging, Segmentation, Address Translation; Page Table; Translation Lookaside Buffer; Page replacement algorithms.	**13**
4	**Advanced Processor Architectures:** Neural Processing Units, unified and on-package memory architectures in laptops, multi-level caches and shared Last Level Cache in desktop CPUs. **Pipelining:** Introduction, Pipeline performance, Hazards: Structural, data, and control hazards, Techniques to resolve hazards. **Parallel Processing:** Parallelism in uniprocessor systems, Multi-core processors, Flynn's taxonomy - SISD, SIMD, MISD, MIMD.	**12**

Text Books				
Sl. No	**Title of the Book**	**Name of the Authors**	**Name of the Publisher**	**Edition & Year**
1	Computer System Architecture	Mano M Morris	Pearson Education	3rd Edition 2017
2	Computer Organization and Architecture: Designing for Performance	William Stallings	Pearson Education,	11/e, 2019
3	Computer Organization and Embedded Systems	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian	McGraw Hill	6/e, 2012

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition & Year**
1	Structured Computer Organization	Andrew S. Tanenbaum, Todd Austin	Pearson Education	6th Edition 2016
2	Computer Organization and Design : The Hardware/ Software Interface: RISC-V Edition	David A. Patterson John L. Hennessy	Morgan Kaufaman	1/e,2018
3	Modern Computer Architecture and Organization	Jim Ledin	Packt Publishing	1/e,2020

Web References/ Video Links (NPTEL, SWAYAM…)	
Sl.No	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105163/
2	https://archive.nptel.ac.in/courses/106/106/106106166/
3	https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/
4	https://nptel.ac.in/courses/106103068/

Course Level Assessment Questions

Course Outcome 1 (CO1):

1. Explain the basic functional units of a computer and describe their interaction during program execution.
2. Differentiate between RISC and CISC architectures with suitable examples.
3. Describe different types of addressing modes used in instruction design
4. Analyze the instruction execution cycle and explain the role of the control unit.
5. Design a simple instruction sequence for addition and conditional branching operations.

Course Outcome 2 (CO2):

1. Explain working of carry look-ahead adder and compare it with ripple carry adder.
2. Demonstrate Booth's algorithm for signed multiplication with an example.
3. Describe the difference between hardwired and microprogrammed control units.
4. Analyze the address sequencing mechanism used in microprogrammed control.
5. Evaluate the advantages and limitations of microprogrammed control

Course Outcome 3 (CO3):

1. Describe the memory hierarchy and explain the trade-offs between cost, capacity, and access time.
2. Explain different cache mapping techniques with suitable diagrams. (Understand)
3. Apply virtual memory to illustrate how paging and segmentation work together.
4. Analyze the function of a Translation Lookaside Buffer (TLB) in address translation.
5. Evaluate the performance of page replacement algorithms

Course Outcome 4 (CO4):

1. Explain Pipelining concept using suitable real life use cases.
2. Describe various types of pipeline hazards and methods to overcome them.
3. Analyze the performance of an instruction pipeline and discuss factors affecting speedup.
4. Compare SISD, SIMD, MISD, and MIMD architectures as per Flynn's classification.
5. Evaluate the role of multi-core processors in achieving parallelism and performance improvement.

Model Question Paper

Reg No.:_____ Name:_____

FEDERAL INSTITUTE OF SCIENCE AND TECHNOLOGY

MCA Integrated S2 (R) Examination, ……(2026 Scheme)

Course Code: 26CAPC2001

Course Name: Computer Organization & Architecture

Max. Marks: 60 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

		CO	Marks
1	Define instruction sequencing. What is straight-line sequencing?	CO1	(3)
2	List different types of instructions with examples.	CO1	(3)
3	What is a carry look-ahead adder?	CO2	(3)
4	Define branching. What is its significance in instruction sequencing?	CO2	(3)
5	Define control memory and address sequencing.	CO3	(3)
6	What are the main fields of an instruction format?	CO3	(3)
7	What is the memory hierarchy?	CO4	(3)
8	What is the role of a Translation Lookaside Buffer (TLB)?	CO4	(3)

PART B

(Answer any one full question from each module, each question carries 9 marks)

Module I

9	a) Explain the basic structure & operation of a computer with block diagram.	CO1	(4)
	b) Explain any five addressing modes used in computers with examples.		(5)
	OR		
10	a) Describe instruction execution cycle with suitable diagram and example.	CO1	(5)
	b) Discuss different instruction types and their execution with examples.		(4)

Module II

11	a) Describe Booth's algorithm for signed multiplication with an example.		(3)
	b) Explain the steps involved in multiplying two positive numbers.	CO2	(3)
	c) Discuss the structure and operation of an ALU		(3)
	OR		
12	a) Explain the design & working of a fast adder using carry look-ahead logic.	CO2	(4)
	b) Realize the minimized expression using logic gates.		(3)

	c) Define a Full Adder. Draw the circuit and truth table.			(2)

Module III

13	a) Explain the structure and functions of the CPU with a neat block diagram.			(5)
	b) Explain how control signals are generated in a microprogrammed control unit.	CO3		(4)

OR

14	a) Explain RISC and CISC architectures with advantages and disadvantages.	CO3		(5)
	b) Describe the steps in the instruction execution cycle.			(4)

Module IV

15	a) Discuss various types of pipeline hazards and techniques to resolve them.	CO4		(9)

OR

16	a) Explain parallel processing concepts and classify computer systems using Flynn's taxonomy.	CO4		(9)

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