Semester 2

Logic Circuit Design

Course Code	Teaching hours per week				Credits	Exam hours	Course Type	CIE Marks	ESE Marks
	L	T	P	R					
26NINPC201	2	1	0	0	3	2.5	Theory	40	60

Preamble: This course provides a fundamental understanding of digital systems and logic circuit design. It introduces number systems, Boolean algebra, digital logic gates, and Boolean expressions as the basis for digital electronics. The course also focuses on the design and implementation of combinational and sequential circuits, while familiarizing students with different logic families. In addition, the course introduces the basics of Verilog HDL for modeling and designing digital systems.

Prerequisites: Nil

Module Number	Syllabus Description	Contact Hours
1	Digital systems - Binary and hexadecimal number systems, Methods of base conversions, Binary and hexadecimal arithmetic, Representation of signed numbers(1's complement, 2's complement,9's complement, 10's complement forms).Fixed and floating point numbers, decimal codes – BCD, Gray codes, Excess 3 code, ASCII code. Boolean Algebra - Basic definitions and axiomatic definition of Boolean algebra , Basic theorems and properties of Boolean algebra, De-Morgan's Theorems ,Boolean functions , canonical and standard forms, Digital logic gates and their truth table. Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS), Karnaugh map Minimization.	11

2	Combinational Logic Systems – Half and full adders, 4 bit ripple carry adder, Subtractors, BCD Adder, Magnitude Comparators, Decoders and Encoders, Multiplexers and De multiplexer. Basic Introduction to Programmable logic devices (PLD) and FPGA. Verilog HDL–Basic language elements, identifiers and operators. Verilog implementation of logic gates and combinational circuits.	11
3	Latches and Flipflops–SR Latch, SR Flipflop, JK, D and T flip flops, Master slave JK FF, Excitation table and characteristic equation, conversion of flipflops. Registers-Shift registers-SIPO, SISO, PISO, PIPO, and Bidirectional. Verilog modeling of flipflops	11
4	Counters- Ripple counter, Mod 10 Counter, Ring counter and Johnsons- Design of Asynchronous and Synchronous counters, Mod N counter, sequence generator. Verilog modeling of asynchronous and synchronous counters. Verilog implementation of sequence generator. Electrical characteristics of TTL and CMOS logic families – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power delay product. TTL inverter -circuit description and operation, CMOS inverter - circuit description and operation, CMOSNAND, CMOS NOR.	11
	Total hours	44

Course Outcomes

At the end of the course students should be able to:

Course Outcome	Description	Bloom Level
CO1	Explain the elements of digital system abstractions such as digital representations of information, digital logic and Boolean algebra	K2
CO2	Design and implement combinational logic circuits	K3

CO3	Design and implement sequential logic circuits	K3
CO4	Design and implement combinational and sequential logic using Verilog HDL	K4
CO5	Compare different logic families	K3

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyze, K5- Evaluate, K6- Create

Mapping of Course Outcomes with Program Outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11
CO1	3	2									
CO2	3	3	3								
CO3	3	3	3								
CO4	3	3	3	2	3						
CO5	3	3									

Text Books

Sl No	Title of Book	Name of Author/s	Publisher	Edition and Year
1	Digital Fundamentals	Thomas L.Flyod	Pearson Education	Edition, 2017
2	Introduction to Logic Circuits and Logic Design with Verilog	Brock J.Lameres	Springer	2nd Edition, 2019

Reference Books

Sl No	Title of Book	Name of Author/s	Publisher	Edition and Year
1	Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog	M Morris Mano, MichaelD. Ciletti	Pearson Education	6th Edition, 2018

2	Digital Design Verilog HDL and fundamentals	Joseph C vanagh	CRC Press	1st Edition, 2008
3	Fundamentals of digital circuits	Kumar A. Anand	PHI	4th Edition, 2016
4	Verilog HDL: A Guide to Digital Design And Synthesis	Samir Palnitkar	Pearson	2nd Edition, 2003

Video Links or any other Reference Materials

Sl No	Details Like Weblink, Publication Details	Module
1	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/	1
2	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/	2
3	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/	3
4	https://archive.nptel.ac.in/courses/117/106/117106086/ https://archive.nptel.ac.in/courses/106/105/106105185/	4

Course Assessment Method (CIE: 60 Marks, ESE: 40 Marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Project	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	30	12.5	12.5	60

Assessment and Evaluation for Project Activity

Sl. No	Evaluation	Allotted Marks
1	Project Planning and Proposal	5

2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
4	Final Presentations & Viva	5
5	Project Quality, Innovation and Creativity	3
Total		**30**

1. Project Planning and Proposal (5 Marks)
    - Clarity and feasibility of the project plan
    - Research and background understanding
    - Defined objectives and methodology
2. Contribution in Progress Presentation and Question Answer Sessions (4 Marks)
    - Individual contribution to the presentation
    - Effectiveness in answering questions and handling feedback
3. Involvement in the Project Work and Team Work (3 Marks)
    - Active participation and individual contribution
    - Teamwork and collaboration
4. Execution and Implementation (10 Marks)
    - Adherence to the project timeline and milestones
    - Application of theoretical knowledge and problem-solving
    - Final Result
5. Final Presentation (5 Marks)
    - Quality and clarity of the overall presentation
    - Individual contribution to the presentation
    - Effectiveness in answering questions
6. Project Quality, Innovation, and Creativity (3 Marks)
    - Overall quality and technical excellence of the project
    - Innovation and originality in the project

- Creativity in solutions and approaches

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions.

Part A	Part B	Total
● 2 Questions from each module. ● Total of 8 Questions, each carrying 2 marks (8x2 =16marks)	● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 2 sub divisions. ● Each question carries 6 marks (4x6 = 24 marks)	40

PBL Course Elements

L: Lecture (3 Hrs.)	R: Project (1 Hr.), 2 Faculty Members		
	Tutorial	Practical	Presentation
Lecture delivery	Project identification	Simulation/ Laboratory Work/ Workshops	Presentation (Progress and Final Presentations)
Group discussion	Project Analysis	Data Collection	Evaluation
Question answer Sessions/ Brainstorming Sessions	Analytical thinking and self-learning	Testing	Project Milestone Reviews, Feedback, Project reformation (If required)
Guest Speakers (Industry Experts)	Case Study/ Field Survey Report	Prototyping	Poster Presentation/ Video Presentation: Students present their results in a 2 to 5 minutes video

MODEL QUESTION PAPER				
FEDERAL INSTITUTE OF SCIENCE AND TECHNOLOGY (AUTONOMOUS) THIRD SEMESTER B.TECH DEGREE EXAMINATION				
LOGIC CIRCUIT DESIGN				
Max Marks: 60			**Duration: 2 Hours 30 minutes**	
PART-A (Answer all Questions, Each Question Carries 3 Marks)				
1		**Convert (202.625)10 to binary.**	**CO1**	**3**
2		**Simplify Y = A + $\bar{A}$ + AB + BC using Boolean algebra.**	**CO1**	**3**
3		**Give Verilog code for a Half Subtractor.**	**CO4**	**3**
4		**Show that an XOR gate is associative.**	**CO2**	**3**
5		**Design a 2-bit decoder**	**CO2**	**3**
6		**Convert a JK flip flop to D and T flip-flops.**	**CO3**	**3**
7		**Define noise margin of a logic gate and explain its significance.**	**CO5**	**3**
8		**Write notes on Emitter Coupled Logic (ECL).**	**CO5**	**3**
PART-B (Answer any one full Question from each Module, Each Question Carries 9 Marks)				
9	**a**	**Represent 543.125 using signed 32-bit floating point representation.**	**CO1**	**5**
	b	**Perform the following operations using 2's complement arithmetic: (i) 111010 - 01101 (ii) 29.625 - 56.5**	**CO1**	**4**
OR				

10	a	Determine the minimal SOP expression for the function: $F(a,b,c,d) = \Sigma m(0,2,4,6,7,8,10,11,12) + d(3,14)$ using Karnaugh maps.	CO1	6
	b	Explain the operators in Verilog.	CO4	3
11	a	Implement the function $F(A,B,C) = AB + B\overline{C} + \overline{A}BC$ using: (i) 8:1 MUX (ii) 4:1 MUX	CO2	6
	b	Realize the function using 3:8 decoder.	CO2	3
		OR		
12	a	Design a Full Adder using NAND gates only.	CO2	6
	b	Write a Verilog code to implement the same.	CO4	3
13	a	Design a synchronous counter using T flip flops that counts through: 0-2-3-7-9-11-15-0-... The counter should reset if any unused state is reached.	CO3	9
		OR		
14	a	Design a Mod-12 synchronous up counter using T flip flops with necessary diagrams.	CO3	9
15	a	Compare TTL & CMOS logic families.	CO5	6
	b	List the applications of CMOS and TTL logic families	CO5	3
OR				
16	a	Define: i) Fan in	CO5	6

		ii) Fan out **iii) Propagation delay**		
	b	**Describe the working of 2 input TTL NAND gate with necessary diagram.**	**CO5**	**3**

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